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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,040	06/28/2006	Mark Alan Lamonte Johnson	297/171 PCT/US	8058
25297	7590	05/15/2008	EXAMINER	
JENKINS, WILSON, TAYLOR & HUNT, P. A. Suite 1200 UNIVERSITY TOWER 3100 TOWER BLVD., DURHAM, NC 27707			KEBEDE, BROOK	
			ART UNIT	PAPER NUMBER
			2823	
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			05/15/2008	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/550,040	JOHNSON ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 27 February 2008.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-50 is/are pending in the application.

4a) Of the above claim(s) 1-14, 17-24, 27-30, 32 and 33 is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 15, 16, 25, 26, 31, 34-40 and 44-50 is/are rejected.

7) Claim(s) 41-43 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 9/21/05; 8/11/06.

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.

5) Notice of Informal Patent Application

6) Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of Group II (Claims 15, 16, 25, 26, 31 and 34-50) in the reply filed on February 27, 2008 is acknowledged.
2. Claims 1-14, 17-24, 27-30, 32 and 33 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on February 27, 2008.

### ***Claim Objections***

3. Claim 15, 16, 25, 26 and 31 are objected to because of the following informalities:  
Claims 15, 16, 25, 26 are linked to the non-elected method claims. Since these claims are withdrawn, claims 15, 16, 25, 26 need to be re-written in order to provide proper antecedent basis and recitation. Claim 31 also objected being dependent of claim 15. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 15, 25, 26, 31, 39 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Lyons et al. (US 6,291,137).**

Re claims 15, 25, 26 and 31, Lyons et al. disclose a FET semiconductor device having a nano-pitched feature (12) formed by edge definition lithography process (see Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Furthermore, patentability of a product does not depend on its method of production. "If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."

*In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Re claim 39, Lyons et al. disclose a semiconductor structure including at least one micrometer-scale feature and at least one nanometer-scale feature being defined using edge definition lithography, the semiconductor structure comprising: a semiconductor substrate (10) ; (b) at least one micrometer-scale feature being located in or on the semiconductor substrate (see Figs. 1 and 2); at least one nanometer-scale feature being (12) located in or on the micrometer-scale feature, the nanometer-scale feature being defined using edge definition lithography (see Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 40, as applied to claim 39 above, Lyons et al. disclose all the claimed limitations including wherein the micrometer- scale feature comprises a channel or hole being defined by the substrate and the nanometer-pitched feature comprises a sidewall (see Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

#### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**7. Claims 34 - 38 and 44 - 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Danzilio (US 6,242,293) in view of Lyons et al. (US 6,291,137)**

Re claim 34, Danzilio discloses a semiconductor structure comprising: a substrate (501) comprising a first layer (510) including a first semiconductor material and a second layer (511) including a second semiconductor material, the first semiconductor material being different from the second semiconductor material.

However, Danzilio does not disclose at least one nanometer-pitched feature being located on the substrate, the nanometer-pitched feature being formed using edge definition lithography.

Lyons et al. disclose at least one nanometer-pitched feature being located on the substrate, the nanometer-pitched feature being formed using edge definition lithography (see Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21). As Lyons et al. disclose, the method of forming one nanometer-pitched feature being located on the substrate, the nanometer-pitched feature being formed using edge definition lithography can be applied to various kinds of devices in order to miniaturize the devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Danzilio reference with one nanometer-

pitched feature being located on the substrate, the nanometer-pitched feature being formed using edge definition lithography as taught by Lyons et al. in order to miniaturize the devices.

Re claim 35, as applied to claim 34 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the nanometer-pitched feature comprises a nanometer-pitched wall located on the first layer (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 36, as applied to claim 35 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the nanometer-pitched wall is formed by a portion of at least one of the first and second layers (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 37, as applied to claim 34 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the nanometer- pitched feature comprises a nanometer-pitched channel formed in a masking material deposited on the substrate (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 38, as applied to claim 37 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the channel extends into at least one of the first and second layers (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 44, Danzilio discloses a field effect transistor having an edge-defined gate, the field effect transistor comprising a substrate including a buffer layer of a first semiconductor material and a channel layer of a second semiconductor material, the second semiconductor material being different from the first semiconductor material; and a gate electrode being located on the substrate between the source and drain electrodes (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

However Danzilio does not disclose the gate electrode being formed using edge definition lithography.

Lyons et al. disclose at least one nanometer-pitched gate electrode being located on the substrate, the gate being formed using edge definition lithography (see Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21). As Lyons et al. disclose, the method of forming one nanometer-pitched feature being located on the substrate, the nanometer-pitched gate electrode being formed using edge definition lithography can be applied to various kinds of devices in order to miniaturize the devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Danzilio reference with one nanometer-pitched feature being located on the substrate, the nanometer-pitched feature being formed using edge definition lithography as taught by Lyons et al. in order to miniaturize the devices.

Re claim 45, as applied to claim 44 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the substrate comprises a donor layer comprising a third semiconductor material being different from the first and second semiconductor materials, the donor layer including a channel, wherein the gate electrode is

located in the channel (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 46, as applied to claim 45 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the channel extends into the channel layer (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 47, as applied to claim 44 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the channel layer includes a channel and the gate electrode is located in the channel (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 48, as applied to claim 44 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the substrate includes a donor layer adjacent to the channel layer and the gate electrode is located on the donor layer (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

Re claim 49, as applied to claim 44 above, Danzilio and Lyons et al. in combination discloses all the claimed limitations including wherein the gate electrode is located on the channel layer (see Danzilio Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21 and Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21).

8. **Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goth et al. (4,400,865) in view of Lyons et al. (US 6,291,137)**

Re claim 50, Goth et al. disclose a bipolar junction transistor comprising: a collector layer; a base layer being adjacent to the collector layer; and emitter being defined on the base layer (see Figs. 9A-9H and related text in Col. 12, line 52 – Col. 14, line 57).

However, Goth et al. do not specifically disclose a nanometer-scale emitter being defined on the base layer using edge definition lithography.

Lyons et al. disclose at least one nanometer-pitched emitter being located on the substrate, the gate being formed using edge definition lithography (see Lyons et al. Figs. 1-5 and related text Col. 3, line 13 - Col. 9, line 21). As Lyons et al. disclose, the method of forming one nanometer-pitched feature being located on the substrate, the nanometer-pitched emitter being formed using edge definition lithography can applied to various kinds of devices in order to miniaturize the devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Goth et al. reference with one nanometer-pitched emitter being located on the substrate, the nanometer-pitched feature being formed using edge definition lithography as taught by Lyons et al. in order to miniaturize the devices.

***Allowable Subject Matter***

9. Claim 41-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Qian (US 5,923,981) also discloses similar inventive subject matter.

***Correspondence***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brook Kebede/  
Primary Examiner, Art Unit 2823

/BK/  
May 12, 2008